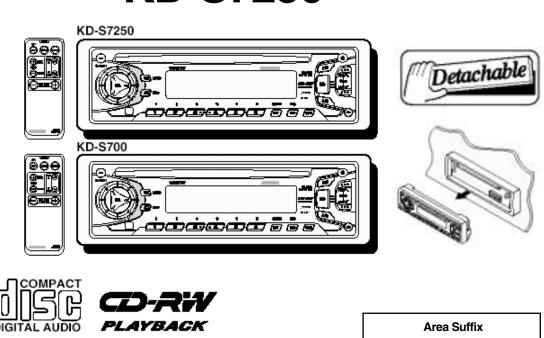


SERVICE MANUAL

CD RECEIVER

KD-S700GN/KD-S700BU KD-S7250



Contents

Safety precaution 1-2	Maintenance of laser pickup 1-14
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Flow of functional	
operation unit TOC read 1-12	

J ----Northern America

Safety precaution

A CAUTION Burrs formed during molding may be left over on some parts of the chassis. Therefore, pay attention to such burrs in the case of preforming repair of this system.

AUTION Please use enough caution not to see the beam directly or touch it in case of an adjustment or operation check.

Preventing static electricity

1. Grounding to prevent damage by static electricity

Electrostatic discharge (ESD), which occurs when static electricity stored in the body, fabric, etc. is discharged, can destroy the laser diode in the traverse unit (optical pickup). Take care to prevent this when performing repairs.

2. About the earth processing for the destruction prevention by static electricity

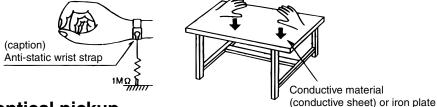
Static electricity in the work area can destroy the optical pickup (laser diode) in devices such as CD players. Be careful to use proper grounding in the area where repairs are being performed.

2-1 Ground the workbench

Ground the workbench by laying conductive material (such as a conductive sheet) or an iron plate over it before placing the traverse unit (optical pickup) on it.

2-2 Ground yourself

Use an anti-static wrist strap to release any static electricity built up in your body.



3. Handling the optical pickup

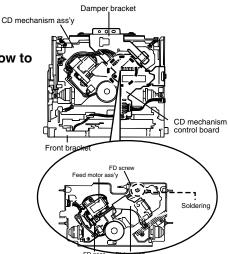
- 1. In order to maintain quality during transport and before installation, both sides of the laser diode on the replacement optical pickup are shorted. After replacement, return the shorted parts to their original condition. (Refer to the text.)
- 2. Do not use a tester to check the condition of the laser diode in the optical pickup. The tester's internal power source can easily destroy the laser diode.

4. Handling the traverse unit (optical pickup)

- 1. Do not subject the traverse unit (optical pickup) to strong shocks, as it is a sensitive, complex unit.
- 2. Cut off the shorted part of the flexible cable using nippers, etc. after replacing the optical pickup. For specific details, refer to the replacement procedure in the text. Remove the anti-static pin when replacing the traverse unit. Be careful not to take too long a time when attaching it to the connector.
- 3. Handle the flexible cable carefully as it may break when subjected to strong force.
- 4. It is not possible to adjust the semi-fixed resistor that adjusts the laser power. Do not turn it

Attention when traverse unit is decomposed

- *Please refer to "Disassembly method" in the text for pick-up and how to detach the substrate.
- Solder is put up before the card wire is removed from connector on the CD substrate as shown in Figure.
 (When the wire is removed without putting up solder, the CD pick-up
 - assembly might destroy.)
- 2.Please remove solder after connecting the card wire with when you install picking up in the substrate.



Disassembly method

<Main body>

■ Removing the front panel assembly (See Fig.1)

1. Press the eject button in the lower right part of the front panel. Remove the front panel assembly from the body.

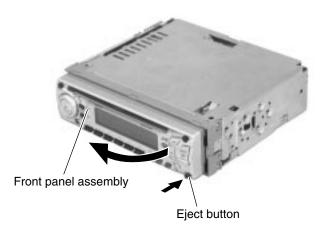


Fig.1

■ Removing the front chassis assembly (See Fig.2 and 3)

- Prior to performing the following procedure, remove the front panel assembly.
- Release the four joint tabs a on both sides of the front chassis assembly and remove the front chassis assembly toward the front.

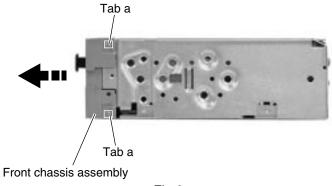
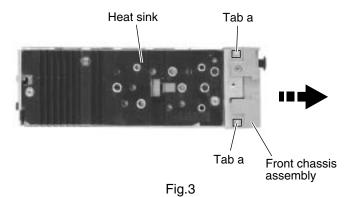
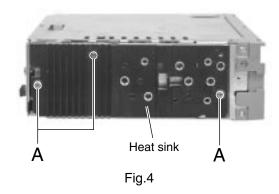


Fig.2



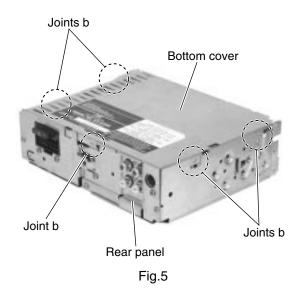
■Removing the heat sink (See Fig.4)

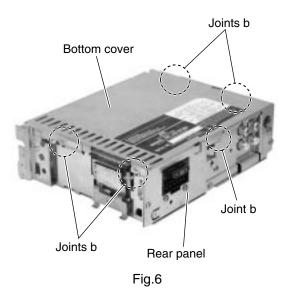
1. Remove the three screws **A** on the left side of the body.



■Removing the bottom cover (See Fig.5 and 6)

- Prior to performing the following procedure, remove the front panel assembly, the front chassis assembly and the heat sink.
- 1. Turn over the body and unjoint the five joints **b** with the bottom cover and the body using a screwdriver.

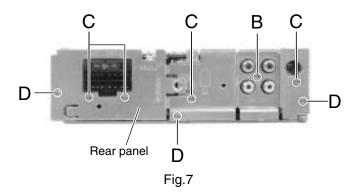


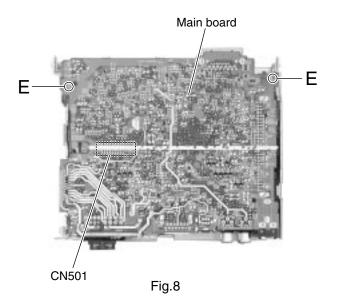


■ Removing the main board

(See Fig.7 and 8)

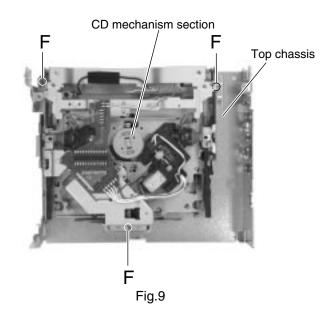
- Prior to performing the following procedure, remove the front panel assembly, the front chassis assembly, the heat sink and the bottom cover.
- 1. Remove the screw **B**, the four screws **C** and the three screws **D** attaching the rear bracket on the back of the body. Remove the rear panel.
- Remove the two screws E attaching the main board on the bottom of the body. Disconnect connector CN501 on the main board in the direction of the arrow.





■ Removing the CD mechanism section (See Fig.9)

- Prior to performing the following procedure, remove the front panel assembly, the front chassis assembly, the heat sink, the bottom cover and the main board.
- 1. Remove the three screws **F** attaching the CD mechanism section on the back of the top chassis.



■ Removing the control switch board (See Fig.10 to 12)

- Prior to performing the following procedure, remove the front panel assembly.
- 1. Remove the four screws **G** attaching the rear cover on the back of the front panel assembly.
- 2. Unjoint the twelve joints ${\bf c}$ with the front panel and the rear cover.
- 3. Remove the control switch board on the back of the front panel.

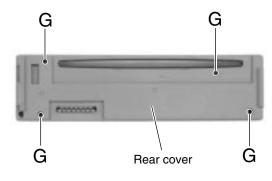


Fig.10

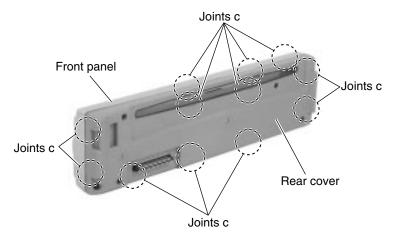


Fig.11

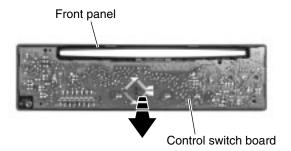


Fig.12

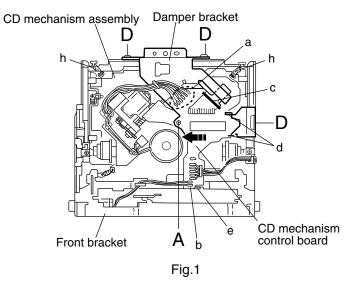
<CD mechanism section>

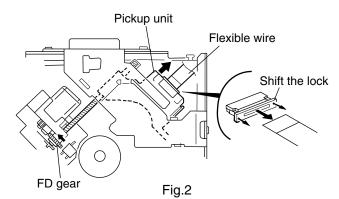
■ Removing the CD mechanism control board (See Fig.1 and 2)

- Unsolder the part a and b on the CD mechanism control board.
- 2. Remove the stator fixing the CD mechanism control board and the damper bracket (To remove the stator smoothly, pick up the center part).
- 3. Remove the screw **A** attaching the CD mechanism control board.
- 4. Remove the CD mechanism control board in the direction of the arrow while releasing it from the two damper bracket slots **d** and the front bracket slot **e**.
- 5. Disconnect the flexible wire from connector on the pickup unit.

ATTENTION: Turn the FD gear in the direction of the arrow to move the entire pickup unit to the appropriate position where the flexible wire of the CD mechanism unit can be disconnected easily.

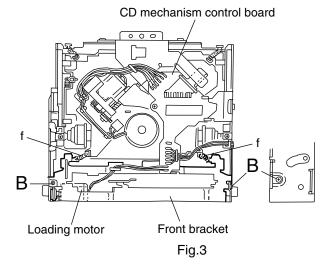
(Refer to Fig.2)

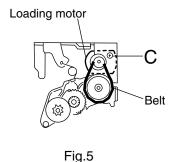


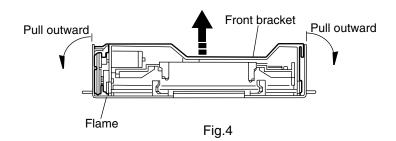


■ Removing the loading motor (See Fig.3 to 5)

- Prior to performing the following procedure, remove the CD mechanism control board.
- 1. Remove the two springs **f** attaching the CD mechanism assembly and the front bracket.
- 2. Remove the two screws **B** and the front bracket while pulling the flame outward.
- 3. Remove the belt and the screw **C** from the loading motor.



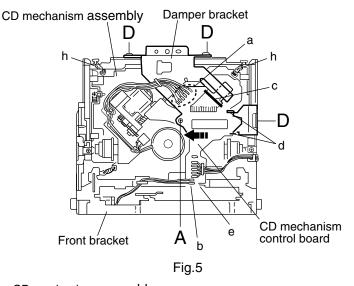


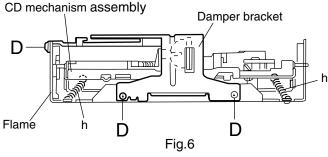


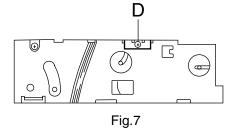
■ Removing the CD mechanism assembly (See Fig.1, 6 to 9)

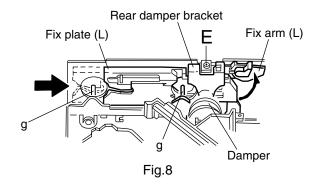
- Prior to performing the following procedure, remove the CD mechanism control board and the front bracket (loading motor).
- Remove the three screws D and the damper bracket.
- 2. Raise the both sides fix arms and move the fix plates in the direction of the arrow to place the four shafts **g** as shown in Fig.8 and 9.
- 3. Remove the CD mechanism assembly and the two springs **h** attaching the flame.
- 4. Remove the two screws E and both sides rear damper brackets from the dampers. Detach the CD mechanism assembly from the left side to the right side.

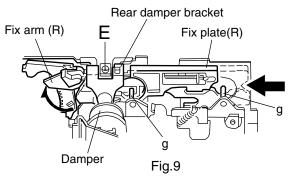
ATTENTION: The CD mechanism assembly can be removed if only the rear damper bracket on the left side is removed.





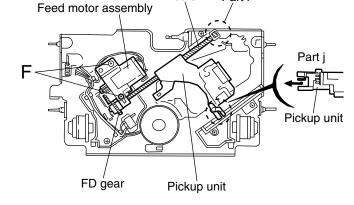






■ Removing the feed motor assembly (See Fig.10)

- Prior to performing the following procedure, remove the CD mechanism control board, the front bracket (loading motor) and the CD mechanism assembly.
- Remove the two screws F and the feed motor assembly.



FD screw

Part i

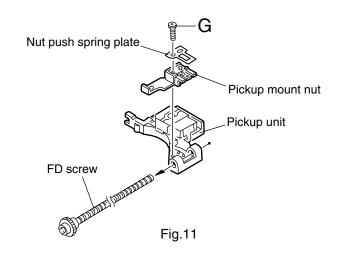
Fig.10

■Removing the pickup unit (See Fig.10 and 11)

- Prior to performing the following procedure, remove the CD mechanism control board, the front bracket (loading motor), the CD mechanism assembly and the feed motor assembly.
- 1. Detach the FD gear part of the pickup unit upward. Then remove the pickup unit while pulling out the part i of the FD screw.

ATTENTION: When reattaching the pickup unit, reattach the part **j** of the pickup unit, then the part **i** of the FD screw.

2. Remove the screw **G** attaching the nut push spring plate and the pickup mount nut from the pickup unit. Pull out the FD screw.



■Removing the spindle motor (See Fig.12 and 13)

- Prior to performing the following procedure, remove the CD mechanism control board, the front bracket (loading motor), the CD mechanism assembly and the feed motor assembly.
- 1. Turn up the CD mechanism assembly and remove the two springs ${\bf k}$ on both sides of the clamper arms. Open the clamper arm upward.
- 2. Turn the turn table, and remove the two screws **H** and the spindle motor.

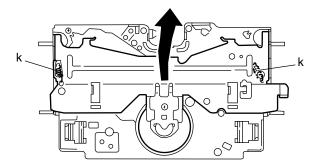
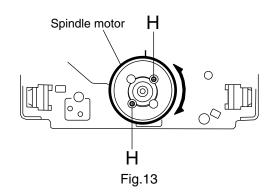


Fig.12



Adjustment method

- Test instruments required for adjustment
 - 1. Digital oscilloscope (100MHz)
 - 2. AM Standard signal generator
 - 3. FM Standard signal generator
 - 4. Stereo modulator
 - 5. Electric voltmeter
 - 6. Digital tester
 - 7. Tracking offset meter
 - 8. Test Disc JVC :CTS-1000
 - 9. Extension cable for check EXTGS004-26P×1

Standard volume position

Balance and Bass &Treble volume: Indication"0"

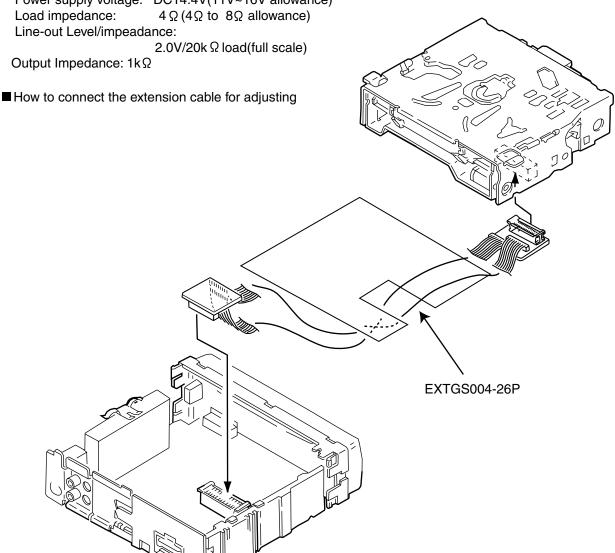
Loudness: OFF : NO BBE BBE Frequency Band

■ FM 87.5MHz ~ 107.9MHz AM 530kHz ~ 1710 kHz

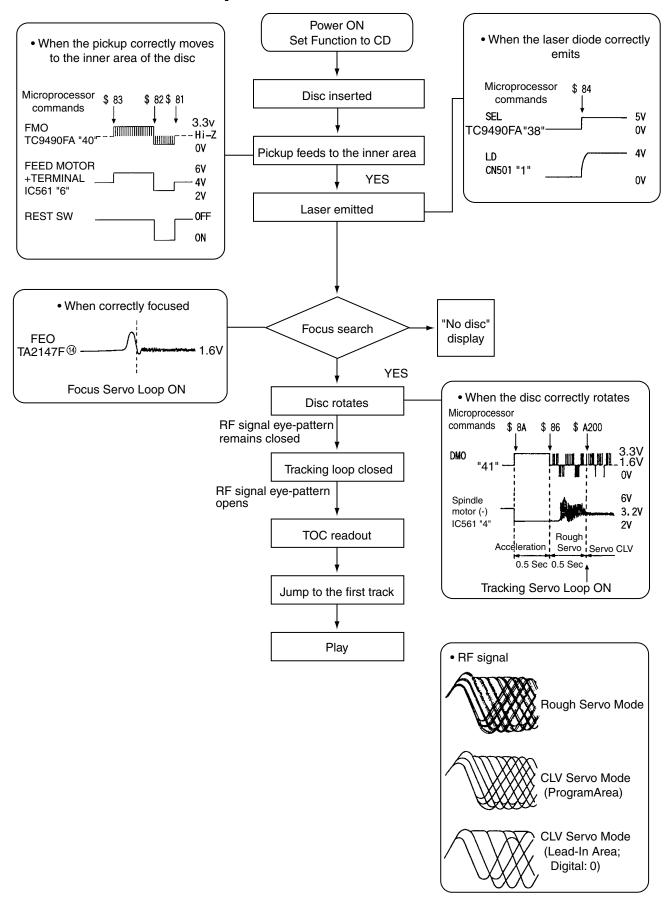
Dummy load

Exclusive dummy load should be used for AM, and FM. For FM dummy load, there is a loss of 6dB between SSG output and antenna input. The loss of 6dB need not be considered since direct reading of figures are applied in this working standard.

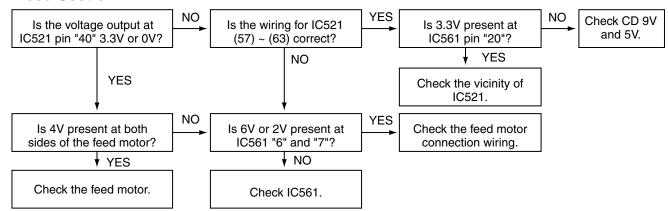
■ Standard measuring conditions Power supply voltage: DC14.4V(11V~16V allowance) Load impedance: $4\Omega (4\Omega \text{ to } 8\Omega \text{ allowance})$ Line-out Level/impeadance: $2.0V/20k \Omega load(full scale)$ Output Impedance: 1kΩ



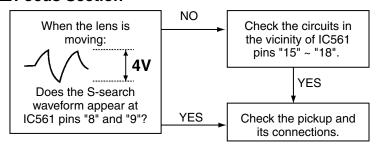
Flow of functional operation until TOC read



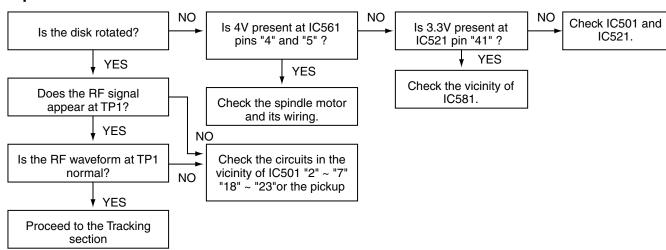
■Feed Section



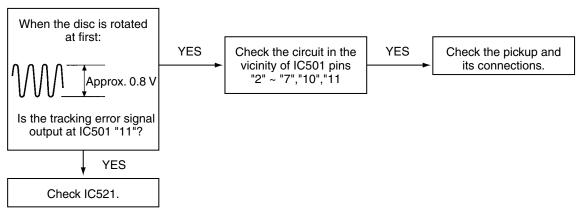
■ Focus Section



■Spindle Section

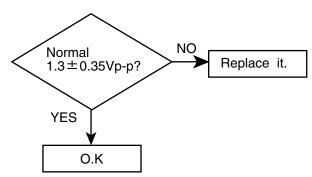


■ Tracking Section



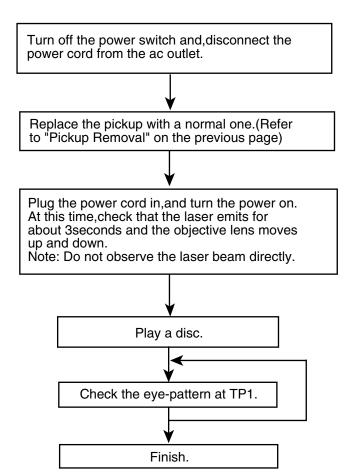
Maintenance of laser pickup

- (1) Cleaning the pick up lens Before you replace the pick up, please try to clean the lens with a alcohol soaked cotton swab.
- (2) Life of the laser diode When the life of the laser diode has expired. the following symptoms will appear.
 (1) The level of RF output (EFM output:ampli
 - tude of eye pattern) will be low.



(3) Semi-fixed resistor on the APC PC board The semi-fixed resistor on the APC printed circuit board which is attached to the pickup is used to adjust the laser power. Since this adjustment should be performed to match the characteristics of the whole optical block, do not touch the semi-fixed resistor. If the laser power is lower than the specified value, the laser diode is almost worn out, and the laser pickup should be replaced. If the semi-fixed resistor is adjusted while the pickup is functioning normally, the laser pickup may be damaged due to excessive current.

Replacement of laser pickup



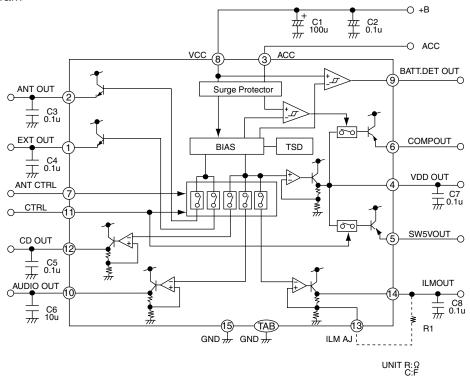
Description of major ICs

■ HA13164A(IC901):Regulator

1.Terminal layout



2.Block diagram

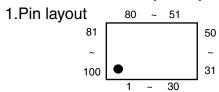


note1) TAB (header of IC) connected to GND

3.Pin function

Pin No.	Symbol	Function	
1	EXTOUT	Output voltage is VCC-1 V when M or H level applied to CTRL pin.	
2	ANTOUT	Output voltage is VCC-1 V when M or H level to CTRL pin and H level	
		to ANT-CTRL.	
3	ACCIN	Connected to ACC.	
4	VDDOUT	Regular 5.7V.	
5	SW5VOUT	Output voltage is 5V when M or H level applied to CTRL pin.	
6	COMPOUT	Output for ACC detector.	
7	ANT CTRL	L:ANT output OFF , H:ANT output ON	
8	VCC	Connected to VCC.	
9	BATT DET	Low battery detect.	
10	AUDIO OUT	Output voltage is 9V when M or H level applied to CTRL pin.	
11	CTRL	L:BIAS OFF, M:BIAS ON, H:CD ON	
12	CD OUT	Output voltage is 8V when H level applied to CTRL pin.	
13	ILM AJ	Adjustment pin for ILM output voltage.	
14	ILM OUT	Output voltage is 10V when M or H level applied to CTRL pin.	
15	GND	Connected to GND.	

■ UPD178078GF-559 (IC701) : System CPU



2.Pin function (1/2)

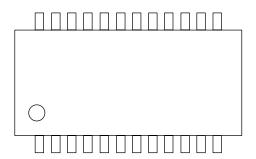
No. Syllido		. –,	1	
2 BUSINT	Pin NO.	Symbol	I/O	FUNCTION
3 BUSSI	1		-	No use
4 BUSSO O JVC bus communication line 5 JBUS-SCK O JVC bus communication line 6,7,8 - No use 9 VOL-DA O Serial data for volume 10 VOL-CLK O Serial clock for volume 11 - No use 12 LCDDA O LCD driver serial data output 13 LCDCLK O Serial data for LCD 14 BUSI/O O JVC bus output select 15 - No use 16 LCDCE O LCD driver communication line 17 SW2 I CD mech switch 18 SW3 I CD mech switch 19 SW4 I CD mech switch 20 RSTSW I Traverse mech rest switch 21 ENC1 I Encoder input 22 ENC2 I Encoder input 23 KEY0 I Key input	2	BUSINT	I	JVC bus communication line
5 JBUS-SCK O JVC bus communication line 6,7,8 - No use 9 VOL-DA O Serial data for volume 10 VOL-CLK O Serial clock for volume 11 - No use 12 LCDDA O LCD driver serial data output 13 LCDCLK O Serial data for LCD 14 BUSI/O O JVC bus output select 15 - No use 16 LCDCE O LCD driver communication line 17 SW2 I CD mech switch 18 SW3 I CD mech switch 19 SW4 I CD mech switch 20 RSTSW I Traverse mech rest switch 21 ENC1 I Encoder input 22 ENC2 I Encoder input 23 KEY0 I Key input 24 KEY1 I Key input 25	3	BUSSI	ı	JVC bus communication line
6,7,8	4	BUSSO	0	JVC bus communication line
9	5	JBUS-SCK	0	JVC bus communication line
10	6,7,8		-	No use
11	9	VOL-DA	0	Serial data for volume
12	10	VOL-CLK	0	Serial clock for volume
13 LCDCLK O Serial data for LCD 14 BUSI/O O JVC bus output select 15 - No use 16 LCDCE O LCD driver communication line 17 SW2 I CD mech switch 18 SW3 I CD mech switch 19 SW4 I CD mech switch 20 RSTSW I Traverse mech rest switch 21 ENC1 I Encoder input 22 ENC2 I Encoder input 23 KEY0 I Key input 24 KEY1 I Key input 25 KEY2 I Key input 26 LEVEL I Audio level input 27 AVDD - Power supply 28 SM I Signal level meter input 29 - No use 30,31 - No use 33 REGCPU - <	11		-	No use
14 BUSI/O O JVC bus output select 15 - No use 16 LCDCE O LCD driver communication line 17 SW2 I CD mech switch 18 SW3 I CD mech switch 19 SW4 I CD mech switch 20 RSTSW I Traverse mech rest switch 21 ENC1 I Encoder input 22 ENC2 I Encoder input 23 KEY0 I Key input 24 KEY1 I Key input 25 KEY2 I Key input 26 LEVEL I Audio level input 27 AVDD - Power supply 28 SM I Signal level meter input 29 - No use 30,31 - No use 32 AVSS - Connect to GND 33 REGCPU - Connect to GND don't	12	LCDDA	0	LCD driver serial data output
15	13	LCDCLK	0	Serial data for LCD
16 LCDCE O LCD driver communication line 17 SW2 I CD mech switch 18 SW3 I CD mech switch 19 SW4 I CD mech switch 20 RSTSW I Traverse mech rest switch 21 ENC1 I Encoder input 22 ENC2 I Encoder input 23 KEY0 I Key input 24 KEY1 I Key input 25 KEY2 I Key input 26 LEVEL I Audio level input 27 AVDD - Power supply 28 SM I Signal level meter input 29 - No use 30,31 - No use 32 AVSS - Connect to GND 33 REGCPU - Connect to GND with capacitor 34 VDD - Power supply 35 REGOSC	14	BUSI/O	0	JVC bus output select
17 SW2	15		-	No use
18 SW3	16	LCDCE	0	LCD driver communication line
19 SW4	17	SW2	I	CD mech switch
20	18	SW3	I	CD mech switch
21 ENC1 I Encoder input 22 ENC2 I Encoder input 23 KEY0 I Key input 24 KEY1 I Key input 25 KEY2 I Key input 26 LEVEL I Audio level input 27 AVDD - Power supply 28 SM I Signal level meter input 29 - No use 30,31 - No use 32 AVSS - Connect to GND 33 REGCPU - Connect to GND with capacitor 34 VDD - Power supply 35 REGOSC - Connect to GND don't have tap 36 X2 - System clock 37 X1 I System clock 38 GND0 - Connect to GND 39 SD/ST I Station detector & Stereo indicator 40 GND2 </td <td>19</td> <td>SW4</td> <td>ı</td> <td>CD mech switch</td>	19	SW4	ı	CD mech switch
22 ENC2 I Encoder input 23 KEY0 I Key input 24 KEY1 I Key input 25 KEY2 I Key input 26 LEVEL I Audio level input 27 AVDD - Power supply 28 SM I Signal level meter input 29 - No use 30,31 - No use 32 AVSS - Connect to GND 33 REGCPU - Connect to GND with capacitor 34 VDD - Power supply 35 REGOSC - Connect to GND don't have tap 36 X2 - System clock 37 X1 I System clock 38 GND0 - Connect to GND 39 SD/ST I Station detector & Stereo indicator 40 GND2 - Connect to GND 41 - <td>20</td> <td>RSTSW</td> <td>ı</td> <td>Traverse mech rest switch</td>	20	RSTSW	ı	Traverse mech rest switch
23 KEY0 I Key input 24 KEY1 I Key input 25 KEY2 I Key input 26 LEVEL I Audio level input 27 AVDD - Power supply 28 SM I Signal level meter input 29 - No use 30,31 - No use 32 AVSS - 33 REGCPU - 34 VDD - 35 REGOSC - 36 X2 - 36 X2 - 37 X1 I 38 GND0 - 39 SD/ST I 40 GND2 - 41 - No use 42 IFC I IF count input 43 VDDPLL -	21	ENC1	I	Encoder input
24 KEY1 I Key input 25 KEY2 I Key input 26 LEVEL I Audio level input 27 AVDD - Power supply 28 SM I Signal level meter input 29 - No use 30,31 - No use 32 AVSS - Connect to GND 33 REGCPU - Connect to GND with capacitor 34 VDD - Power supply 35 REGOSC - Connect to GND don't have tap 36 X2 - System clock 37 X1 I System clock 38 GND0 - Connect to GND 39 SD/ST I Station detector & Stereo indicator 40 GND2 - Connect to GND 41 - No use 42 IFC I IF count input 43 VDDPLL -	22	ENC2	I	Encoder input
25 KEY2 I Key input 26 LEVEL I Audio level input 27 AVDD - Power supply 28 SM I Signal level meter input 29 - No use 30,31 - No use 32 AVSS - Connect to GND 33 REGCPU - Connect to GND with capacitor 34 VDD - Power supply 35 REGOSC - Connect to GND don't have tap 36 X2 - System clock 37 X1 I System clock 38 GND0 - Connect to GND 39 SD/ST I Station detector & Stereo indicator 40 GND2 - Connect to GND 41 - No use 42 IFC I IF count input 43 VDDPLL -	23	KEY0	ı	Key input
26 LEVEL I Audio level input 27 AVDD - Power supply 28 SM I Signal level meter input 29 - No use 30,31 - No use 32 AVSS - Connect to GND 33 REGCPU - Connect to GND with capacitor 34 VDD - Power supply 35 REGOSC - Connect to GND don't have tap 36 X2 - System clock 37 X1 I System clock 38 GND0 - Connect to GND 39 SD/ST I Station detector & Stereo indicator 40 GND2 - Connect to GND 41 - No use 42 IFC I IF count input 43 VDDPLL -	24	KEY1	I	Key input
27 AVDD - Power supply 28 SM I Signal level meter input 29 - No use 30,31 - No use 32 AVSS - Connect to GND 33 REGCPU - Connect to GND with capacitor 34 VDD - Power supply 35 REGOSC - Connect to GND don't have tap 36 X2 - System clock 37 X1 I System clock 38 GND0 - Connect to GND 39 SD/ST I Station detector & Stereo indicator 40 GND2 - Connect to GND 41 - No use 42 IFC I IF count input 43 VDDPLL -	25	KEY2	I	Key input
28 SM I Signal level meter input 29 - No use 30,31 - No use 32 AVSS - Connect to GND 33 REGCPU - Connect to GND with capacitor 34 VDD - Power supply 35 REGOSC - Connect to GND don't have tap 36 X2 - System clock 37 X1 I System clock 38 GND0 - Connect to GND 39 SD/ST I Station detector & Stereo indicator 40 GND2 - Connect to GND 41 - No use 42 IFC I IF count input 43 VDDPLL -	26	LEVEL	I	Audio level input
29 - No use 30,31 - No use 32 AVSS - Connect to GND 33 REGCPU - Connect to GND with capacitor 34 VDD - Power supply 35 REGOSC - Connect to GND don't have tap 36 X2 - System clock 37 X1 I System clock 38 GND0 - Connect to GND 39 SD/ST I Station detector & Stereo indicator 40 GND2 - Connect to GND 41 - No use 42 IFC I IF count input 43 VDDPLL	27	AVDD	-	Power supply
30,31 - No use 32 AVSS - Connect to GND 33 REGCPU - Connect to GND with capacitor 34 VDD - Power supply 35 REGOSC - Connect to GND don't have tap 36 X2 - System clock 37 X1 I System clock 38 GND0 - Connect to GND 39 SD/ST I Station detector & Stereo indicator 40 GND2 - Connect to GND 41 - No use 42 IFC I IF count input 43 VDDPLL -	28	SM	I	Signal level meter input
32 AVSS - Connect to GND 33 REGCPU - Connect to GND with capacitor 34 VDD - Power supply 35 REGOSC - Connect to GND don't have tap 36 X2 - System clock 37 X1 I System clock 38 GND0 - Connect to GND 39 SD/ST I Station detector & Stereo indicator 40 GND2 - Connect to GND 41 - No use 42 IFC I IF count input 43 VDDPLL -	29		-	No use
33 REGCPU - Connect to GND with capacitor 34 VDD - Power supply 35 REGOSC - Connect to GND don't have tap 36 X2 - System clock 37 X1 I System clock 38 GND0 - Connect to GND 39 SD/ST I Station detector & Stereo indicator 40 GND2 - Connect to GND 41 - No use 42 IFC I IF count input 43 VDDPLL -	30,31		-	No use
34 VDD - Power supply 35 REGOSC - Connect to GND don't have tap 36 X2 - System clock 37 X1 I System clock 38 GND0 - Connect to GND 39 SD/ST I Station detector & Stereo indicator 40 GND2 - Connect to GND 41 - No use 42 IFC I IF count input 43 VDDPLL -	32	AVSS	-	Connect to GND
35 REGOSC - Connect to GND don't have tap 36 X2 - System clock 37 X1 I System clock 38 GND0 - Connect to GND 39 SD/ST I Station detector & Stereo indicator 40 GND2 - Connect to GND 41 - No use 42 IFC I IF count input 43 VDDPLL -	33	REGCPU	-	Connect to GND with capacitor
36 X2 - System clock 37 X1 I System clock 38 GND0 - Connect to GND 39 SD/ST I Station detector & Stereo indicator 40 GND2 - Connect to GND 41 - No use 42 IFC I IF count input 43 VDDPLL -	34	VDD	-	Power supply
37 X1 I System clock 38 GND0 - Connect to GND 39 SD/ST I Station detector & Stereo indicator 40 GND2 - Connect to GND 41 - No use 42 IFC I IF count input 43 VDDPLL -	35	REGOSC	-	Connect to GND don't have tap
37 X1 I System clock 38 GND0 - Connect to GND 39 SD/ST I Station detector & Stereo indicator 40 GND2 - Connect to GND 41 - No use 42 IFC I IF count input 43 VDDPLL -	36	X2	-	System clock
39 SD/ST I Station detector & Stereo indicator 40 GND2 - Connect to GND 41 - No use 42 IFC I IF count input 43 VDDPLL -	37	X1	I	
40 GND2 - Connect to GND 41 - No use 42 IFC I IF count input 43 VDDPLL -	38	GND0	-	•
40 GND2 - Connect to GND 41 - No use 42 IFC I IF count input 43 VDDPLL -	39	SD/ST	ı	Station detector & Stereo indicator
42 IFC I IF count input 43 VDDPLL	40	GND2	-	Connect to GND
43 VDDPLL	41		-	No use
	42	IFC	I	IF count input
	43	VDDPLL	-	
44 OSC I FM,AM osc input	44	OSC	I	FM,AM osc input
45 - No use	45		-	No use

2.Pin function (2/2)

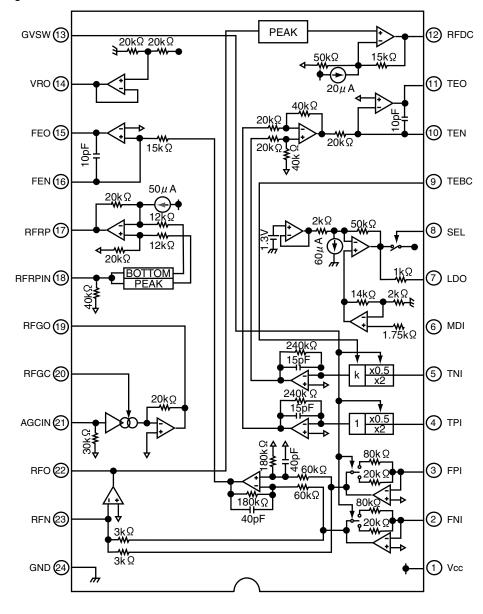
Pin NO.	Symbol	I/O	FUNCTION
46	GNDPLL	-	
47	AMEO	0	PLL error output for AM
48	FMEO	0	PLL error output for FM
49	IC(VPP)	-	Setting to write for flash
50	RESET	ı	System reset
51	SW1	I	CD mech switch
52	REMOCON	ı	Remocon input
53	VTR-LOGIC	-	No use
54	VR-CONT	-	No use
55	POWER	0	Power control
56	CDON	0	CD power control
57	MUTE	0	Mute control
58	STAGE	-	No use
59	BUZZER	-	No use
60	JAPAN	-	No use
61~67		-	No use
68	CDRW	0	CD-RW detect signal output
69	LM0	0	CD mech driver control
70	LM1	0	CD mech driver control
71	BUCK	0	CD LSI communication line
72	CCE	0	CD LSI communication line
73	BUS0	I/O	CD LSI communication line
74	BUS1	I/O	CD LSI communication line
75	BUS2	I/O	CD LSI communication line
76	BUS3	I/O	CD LSI communication line
77	RST	0	CD LSI communication line
78	PS1	ı	ACC detection input
79	PS2	ı	Memory detection
80	DETACH	ı	Detach detection
81		-	No use
82	GND1	-	Connect to GND
83	MONO	0	Mono by force
84	SEEK/STOP	0	Switching SEEK & STOP
85	FM/AM	0	Band switch
86		-	No use
87	ANT	0	Antena regulator control signal
88	TEL MUTE	-	No use
89~98	NC	-	Non connection
99	VDDPORT	-	Vdd
100	GNDPORT	-	Connect to GND

■ TA2147F-X(IC501):RF AMP

1.Terminal layout



2.Block diagram



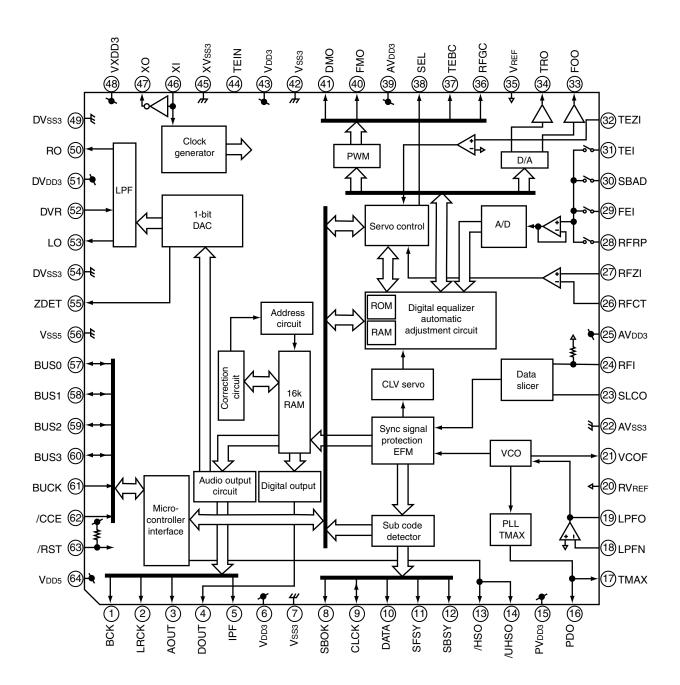
3.Pin function

TA2147F-X

D: N		1/0	TA2147F-X				
Pin No.	Symbol	I/O	Function				
1	Vcc	-	3.3V Power supply pin				
2	FNI	ı	Main-beam amp input pin				
3	FPI	!	Main-beam amp input pin				
4	TPI		Sub-beam amp input pin				
5	TNI	<u> </u>	Sub-beam input pin				
6	MDI		Monitor photo diode amp input pin				
7	LDO	0	Laser diode amp output pin				
8	SEL	I	APC circuit ON/OFF control signal, laser diode (LDO) control signal input or bottom/peak detection frequency change pin.				
			SEL APC LDO				
			GND OFF Connected to Vcc through 1kΩresistor				
			HIZ ON Control signal output				
			Vcc ON Control signal output				
9	TEBC	I	Tracking error balance adjustment signal pin				
			Adjusts TE signal balance by eliminating carrier component from				
			PWM signal(3-state output, PWM carrier = 88.2kHz) output from				
			TC9490F/FA TEBC pin using RC-LPF and inputting DC.				
			TEBC input voltage:GND~Vcc				
10	TEN	I	Tracking error signal generation amp negative-phase input pin				
11	TEO	0	Tracking error signal generation amp output pin.				
			Combining TEO signal and RFRP signal with TC9490F/FA configures				
			tracking search system.				
12	RFDC	0	RF signal peak detection output pin				
13	GVSW	ı	AGC/FE/TE amp gain change pin				
			GVSW Mode				
			GND CD-RW				
			HIZ CD-DA				
			Vcc CD-DA				
<u> </u>		_					
14	VRO	0	Reference voltage (VRO) output pin *VRO = 1/2 Vcc when Vcc = 3.3V				
15	FEO	0	Focus error signal generation amp output pin				
16	FEN		Focus error signal generation amp negative-phase input pin				
17	RFRP	0	Signal amp output pin for track count				
			Combining RFRP signal TEO signal with TC9490F/FA configures tracking				
			search system.				
10	DEDDIN		Circular appropriate annual manual min for two streets				
18	RFRPIN	1	Signal generation amp input pin for track count				
19	RFGO	0	RF signal amplitude adjustment amp output pin				
20	RFGC	'	RF amplitude adjustment control signal input pin				
			Adjusts RF signal amplitude by eliminating carrier component from PWM				
			signal (3-state output, PWM carrier = 88.2kHz) output from TC9490F/FA				
			RFGC pin using RC-LPF and inputting DC.				
21	AGCIN	ı	*RFGC input voltage : GND-Vcc				
	<u> </u>		RF signal amplitude adjustment amp input pin				
22	RFO	0	RF signal generation amp output pin				
23	RFN	1	RF signal generation amp input pin				
24	GND	-	GND pin				

■TC9490FA(IC521):DSP&DAC

1.Terminal layout & block daiagram



2.Pin function

TC9490FA(2/3)

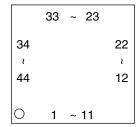
	1				TC9490FA(2/3)
Pin No.	Symbol	I/O	Function		
1	BCK	0	Bit clock outputpin 32fs, 48fs, or 64fs selectable by command.		
2	LRCK	0	L/R channel clock output pin."L" for L channe and "H" for R channel.		
			Output polarity can be inverted by command.		
3	AOUT	0	Audio data output pin. N	/ISB-first o	or LSB-first selectable by command.
4	DOUT	0			p to double-speed playback.
5	IPF	0	Correction flag output pin.When set to "H",AOUT output cannot be corrected		
			by C2 correction proces	ssing.	
6	VDD3	-	Digital 3.3V power supp	ly voltage	pin.
7	VSS3	-	Digital GND pin.		
8	SBOK	0	Subcode Q data CRCC result output pin."H" level when result is OK.		
9	CLCK	I/O	Subcode P-W data read	d clockI/O	pin. I/O polarity selectable by command.
10	DATA	0	Subcode P-W data outp	out pin.	
11	SFSY	0	Playback frame sync sig	gnal outpu	ut pin.
12	SBSY	0	•	<u> </u>	t pin. "H" level at S1 when subcode sync is
			detected.		
13	/HSO	0	Playback speed mode f	lag output	t pins.
			, ,	5 1	•
			/UHSO /HSO	Playba	ck speed
14	/UHSO	0	701100 71100	<u> </u>	<u> </u>
			H H		rmal
			H L	Do	uble
			L L	4 ti	mes
				-	
15	PVDD3	-	PLL-only 3.3V power su	stlov vlaar	age pin.
16	PDO	0	EFM and PLCK phase		-
17	TMAX	Ō	TMAX detection result output pin.		
			TMAX Detection result TMAX Output		
			Longer than fixed	period	"PVDD3"
			Within fixed per		"HIZ"
			Shorter than fixed		"AVss3"
			Onortor triarring	ponou	714000
18	LPFN		Inverted input pin for PL	L LPF an	np.
19	LPFO	0	Output oin for PLL LPF		
20	PVREF	_	PLL-only VREF pin.		
21	VCOF	0	VCO filter pin.		
22	AVss3	_	Analog GND pin.		
23	SLCO	0	DAC output pin for data	slice leve	el generation.
24	RFI	ı	RF signal input pin.Zin s		
25	AV	-	Analog 3.3V power supply voltage pin.		
26	RFCT		RFRP signal center level input pin.		
27	RFZI		RFRP signal zero-cross input pin.		
28	RFRP	i	RF ripple signal input pin.		
29	FEI	i	Focus error signal input pin.		
30	SBAD	l i	Sub-beam adder signal input pin.		
31	TEI	i i	Tracking error input pin. Inputs when tracking servo is on.		
32	TEZI	l i	Tracking error signal zero-cross input pin.		
33	FOO	0	Focus equalizer output		ikar kun
34	TRO	0	Tracking equalizer output		
35	VREF		Analog reference power		oltage nin
	I AUEL		, trialog reference power	Guppiy V	onago piii.

2.Pin function

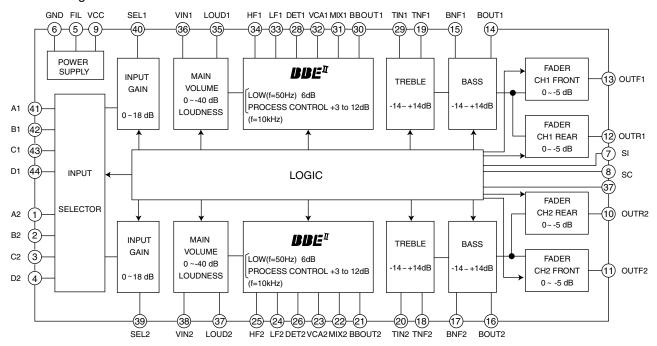
TC9490FA(3/3) I/O Pin No. Symbol **Function** 36 **RFGC** 0 RF amplitude adjustment control signal output pin. 37 **TEBC** Tracking balance control signal output pin. 0 APC circuit ON/OFF signal output pin. At laser on,high impedance with 38 SEL 0 UHS="L", H output with UHS="H". 39 **AV**DD3 Analog 3.3V power supply voltage pin. 40 FMO O Feed equalizer output pin. DMO 41 0 Disc equalizer output pin. Digital GND pin. 42 Vss3 Digital 3.3V power supply voltage pin. 43 V_{DD3} 44 TESIN Test input pin. Normally, fixed to "L". I XVss3 System clock oscillator GND pin. 45 46 ΧI ı System clock oscilatoe input pin. XO 47 0 System clock oscillator output pin. XV_{DD3} System clock oscillator 3.3V power supply voltage pin. 48 49 DVss3 DA converter GND pin. 50 RO 0 R-channel data forward output pin. 51 DV_{DD3} DA converter 3.3V power supply pin. 52 DVR Reference voltage pin. LO 0 L-channel data forward output pin. 53 54 DVss3 DA converter GND pin. 0 **ZDET** 1 bit DA converter zero data detection flag output pin. 55 56 VSS5 -Microcontroller interface GND pin. BUS₀ 57 I/O Microcontroller interface data I/O pins. 58 BUS1 59 BUS2 BUS3 60 BUCK Microcontroller interface clock input pin. 61 1 62 /CCE Microcontroller interface chip enable signal input pin.At "L". Bus0 to BUS3 are active. Reset signal input pin. At reset,"L". /RST 63 64 V_{DD5} Microcontroller interface 5V power supply pin.

■ BD3860K (IC161):E.Vol&LOUD

1.Terminal layout



2.Block diagram

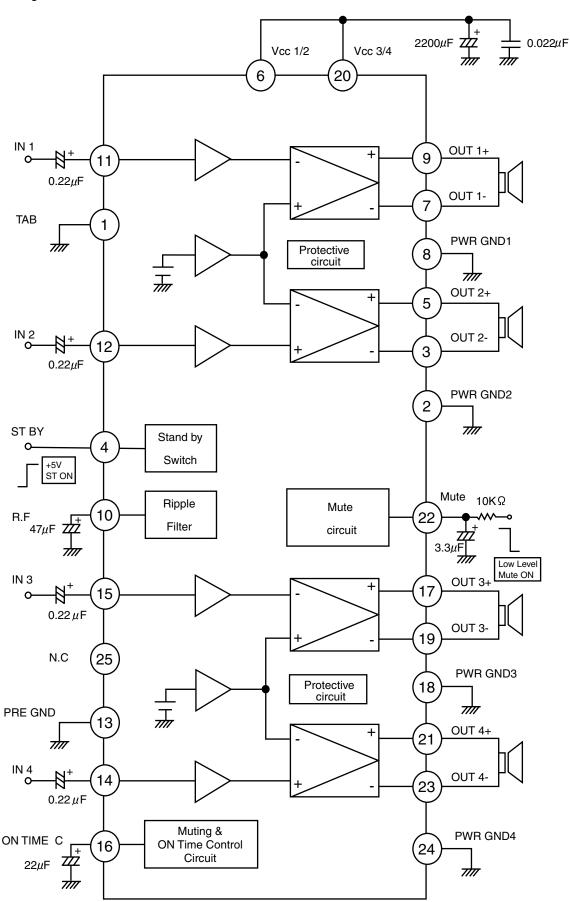


3.Pin function

٥.	5.FIII IUIICIIOII						
Pin No.	Symbol	Function	Pin No.	Symbol	Function		
1	A2	CH2 Input Pin A	23	VCA2	CH2 High Pass VCA Output Pin		
2	B2	CH2 Input Pin B	24	LF2	CH2 Low Pass Filter Setting Pin		
3	C2	CH2 Input Pin C	25	HF2	CH2 High Pass Filter Setting Pin		
4	D2	CH2 Input Pin D	26	DET2	CH2 High Pass Attack/Release Time Setting Pin		
5	FIL	1/2 VCC Pin	27	DEF	BBE II ON/OFF switching time constant pin		
6	GND	Ground Pin	28	DET1	CH1 High Pass Attack/Release Time Setting Pin		
7	SI	Serial Data Receiving Pin	29	TIN1	CH1 treble Input Pin		
8	SC	Serial Clock Receiving Pin	30	BBOUT1	CH1 BBE II Signal Output Pin		
9	VCC	Power Supply Pin	31	MIX1	CH1 Output MIX Amplifier Inverse Input Pin		
10	OUTR2	CH2 Rear Output Pin	32	VCA1	CH1 High Pass VCA Output Pin		
11	OUTF2	CH2 Front Output Pin	33	LF1	CH1 Low Pass Filter Setting Pin		
12	OUTR1	CH1 Rear Output Pin	34	HF1	CH1 High Pass Filter Setting Pin		
13	OUTF1	CH1 Front Output Pin	35	LOUD1	CH1 Loudness Filter Setting Pin		
14	BOUT1	CH1 Bass Filter Setting Pin	36	VIN1	CH1 Main Volume Input Pin		
15	BNF1	CH1 Bass Filter Setting Pin	37	LOUD2	CH2 Loudness Filter setting Pin		
16	BOUT2	CH2 Bass Filter Setting Pin	38	VIN2	CH2 Main Volume Input Pin		
17	BNF2	CH2 Bass Filter Setting Pin	39	SEL2	CH2 Input Gain Output Pin		
18	TNF2	CH2 Treble Filter Setting Pin	40	SEL1	CH1 Input Gain output Pin		
19	TNF1	CH1 Treble Filter Setting Pin	41	A1	CH1 Input Pin A		
20	TIN2	CH2 Treble Input Pin	42	B1	CH1 Input Pin B		
21	BBOUT2	CH2 BBE II Signal Output Pin	43	C1	CH1 Input Pin C		
22	MIX2	CH2 Output MIX Amplifier	44	D1	CH1 Input Pin D		
		Inverse Input Pin					

■LA4743K(IC302):Power AMP

1.Block diagram



2.Terminal layout

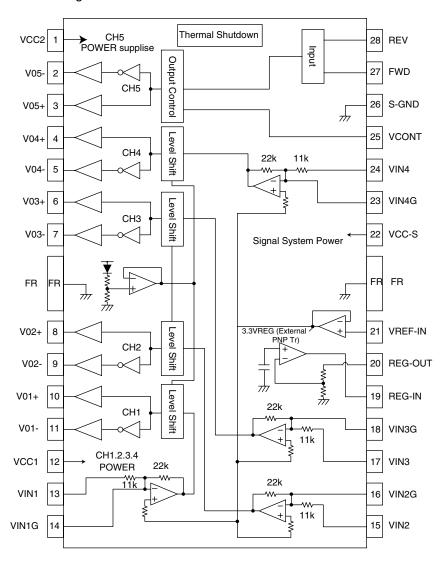


3.Pin function

Pin No.	Symbol	Function
1	TAB	Header of IC
2	GND	Power GND
3	RFO-	Outpur(-) for front Rch
4	STBY	Stand by input
5	RFO+	Output (+) for front Rch
6	VCC1/2	Power input
7	RRO-	Output (-) for rear Rch
8	GND	Power GND
9	RRO+	Output (+) for rear Rch
10	VREF	Ripple filter
11	RRIN	Rear Rch input
12	RFIN	Front Rch input
13	SGND	Signal GND
14	LFIN	Front Lch input
15	LRIN	Rear Lch input
16	ONTIME	Power on time control
17	LRO+	Output (+) for rear Lch
18	GND	Power GND
19	LRO-	Output (-) for rear Lch
20	VCC3/4	Power input
21	LFO+	Output (+) for front
22	MUTE	Muting control input
23	LFO-GND	1 ()
24	NC	Power GND
25		No connection

■LA6574H-X (IC561) :CD driver

1.Terminal layout & brock daiagram

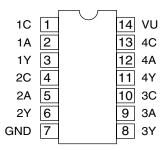


2.Pin function

	ı				
Pin No.	Symbol	Function	Pin No.	Symbol	Function
1	VCC2	CH5 power supplies.	15	VIN2	CH2 input terminal
2	VO5-	Loading output(-)	16	VIN2G	CH2 input terminal(for gain adjustment)
3	VO5+	Loading output(+)	17	VIN3	CH3 input terminal
4	VO4+	CH4 output terminal(+)	18	VIN3G	CH3 input terminal(for gain adjustment)
5	VO4-	CH4 output terminal(-)	19	REG-IN	Regulator terminal
6	VO3+	CH3 output terminal(+)	20	REG-OUT	Regulator terminal
7	VO3-	CH3 output terminal(-)	21	VREF-IN	Standard voltage input terminal
8	VO2+	CH2 output terminal(+)	22	VCC-S	Signal system power
9	VO2-	CH2 output terminal(-)	23	VIN4G	CH4 input terminal(for gain adjustment)
10	VO1+	CH1 output terminal(+)	24	VIN4	CH4 input terminal
11	VO1-	CH1 output terminal(-)	25	VCONT	CH5 output voltage set terminal
12	VCC1	CH1,2,3,4 power supplies	26	S-GND	Signal system GND
13	VIN1	CH1 input terminal	27	FWD	CH5 output switch terminal
14	VIN1G	CH1 input terminal		REV	CH5 output switch terminal
		(for gain adjustment)			

■ HD74HC126FP-X (IC801) : Buffer

1.Terminal layout

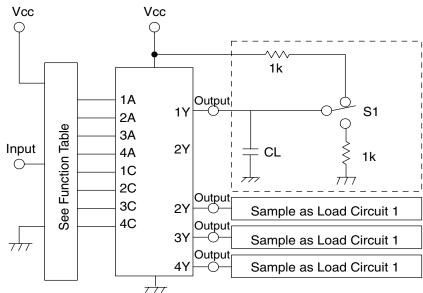


3.Pin function

Inp	ut	Output
С	Α	Υ
L	Х	Z
Н	L	Н
Н	Н	L

Note) H:High level L:Low level X:Irrelevant Z:Off(High-impedance) State a 3-state input

2.Block diagram



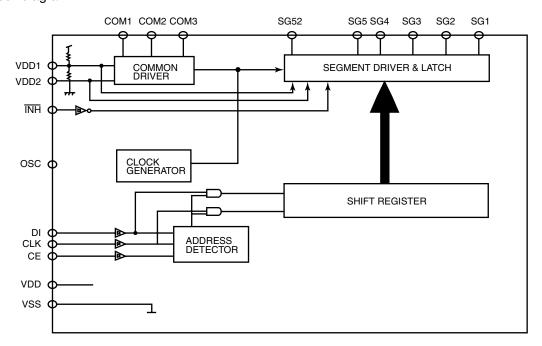
Note) CL includes probe and jig capacitance

■ PT6523LQ(IC601):LCD DRIVER

1.Pin layout



2.Block diagram

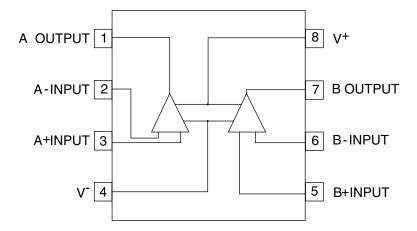


3.Pin function

Dia Na	D'a Nama	1/0	D
Pin No.	Pin Name	I/O	Description
1 ~ 52	SG1 ~ SG52	0	Segment output pins
53 ~ 55	COM1 ~ COM3	0	Common driver output pins
56	VDD	-	Power supply
57	ĪNH	I	Display OFF control input pin. When this pin is "LOW", the display is forcibly/turned OFF. (SG1 to SG52, COM1 to COM3 are set to "LOW"). When this pin is set to "High", the display is ON. (See Note 1*)
58	VDD1	I	Used for the 2/3 bias voltage when the bias voltages are provided externally. Connect to VDD2 when 1/2 bias is used.
59	VDD2	I	Used for 1/3 bias voltage when the bias voltages are provided externally. Connect to VDD1 when 1/2 bias used.
60	VSS	-	Ground pin
61	OSC	I/O	Oscillation Input/Output pin
62	CE	I	Chip enable pin
63	CLK	I	Synchronization clock
64	DI	I	Transfer data pin

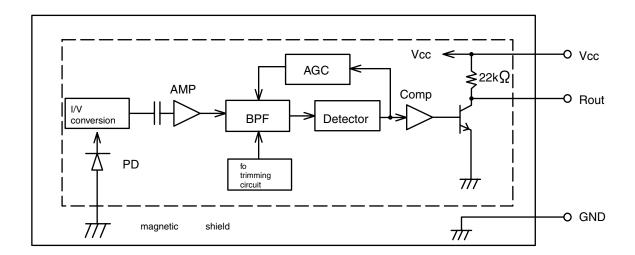
*Note 1: When $\overline{\text{INH}} = \text{"LOW"}$: Serial data transfers can be performed when the display is forcibly OFF.

■ NJM4565M-WE (IC571) : Ope. amp



■ RPM6938-SV4(IC602) : Remote sensor

1.Block diagram





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